Hi3110QV100 Demodulating and Decoding Chip

Features

High-Performance ARM926EJ-S Core
- 4 KB I-Cache, 4 KB D-Cache, and 2 KB TCM
- Processing performance: 270 MIPS@252 MHz
- JAVA or DSP accelerator

QAM
- 16/32/64/128/256-QAM demodulation
- Compliant with the DVB-C, ITU J83-A and ITU J83-C stream specifications
- An Integrated high performance 10-bit IF ADC, intended for all direct IF QAM solutions
- All digital demodulation
- Support for variable symbol rates from 0.87 Mbaud to 9 Mbaud
- On-chip timing and carrier recovery; 400 ppm maximum clock deviation; 400 kHz maximum frequency deviation
- Automatic bandwidth select matched filtering, with the raised cosine roll down factor of 0.15 or 0.13
- An adaptive channel equalizer that requires no training sequence, offering blind equalization and decision feedback equalization
- Internal registers controlled and monitored through the two-wire bus
- Reed Solomon (RS) (204, 188, 8) forward error correction, which can be masked
- Dual automatic gain controls (AGCs)
- Real-time monitoring of signal quality
- Interrupt generation
- Chip status indicator
- The system clock can be generated on chip through external oscillators
- Programmable output clock
- Serial and parallel Transport Stream (TS) output
- Convolutional deinterleaving with depth 12
- Dedifferential encoding, demapping and descrambling functions

Transport DEMUX
- Serial and parallel input interfaces, 96 Mbit/s in serial mode, 13.5 MB/s in parallel mode
- 32 PID filtering channels
- AF information output to Channel 33
- 32 PES/Section data filters
- Common DVB descrambler
- Integrated clock recovery module
- TS data output to 33 cyclic buffers

MCE
- Audio decoder start and decoding control
- Sampling rate update of the audio decoder and handling of decoding exceptions
- Video decoder start and decoding control
- Handling of video decoding exceptions
- Support for the VO start, display parameter update, and adaptive NTSC/PAL output
- Handling of the exceptions in the VO parameters
- Working together with the CPU to synchronize video and audio processing

Audio Decoder
- Audio ES and PES decoding
- MPEG-1 layer I/II and MPEG-2 layer I/II decoding
- PCM channel and MP3 soft decompression
- PCM channels that support PCM and bypass output of other digital audio data
- Sampling rates of 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz and 48 kHz
- Integrated audio DAC with 24-bit precision; support for dual audio channel output
- I^2S bypass output interface
- S/PDIF digital output
- Audio setting by selecting left/right audio channel (s)
- Mute mode
- Mono audio channels mapped to dual audio channels

Video Decoder
- Video ES and PES decoding
- MPEG-1 bit stream decoding
- MP@ML (and lower) MPEG-2 bit streams decoding
- Compatible with input streams whose bit rate is 15 Mbit/s or lower
- 24 fps to 30 fps frame rate
- Frame image specifications: 720 × 480 pixels (30 Hz), 720 × 576 pixels (25 Hz)
- Video formats: progressive, interlaced, support for frame encoding and field encoding in the interlaced mode
- User data extraction
- Error detection and error recovery

VO
- Five-layer display, including Background, Video, Still, On-Screen Display (OSD), and Cursor
- High-performance 2D graphics acceleration, offering high quality picture design and supporting transparent copy
- Video arbitrary scaling
- Forced video format conversion between PAL and NTSC
- Multiple OSD regions based on linked-list structure
- OSD image format: 256-color mode, 16-bit direct color mode, or 32-bit direct color mode
- RGB color mode
- OSD image conversion between PAL and NTSC
- OSD support for antiflicker filter
- 16-color and 32 x 32 pixels cursor display mode
- Write-back of displayed video graphics

Mixer/Encoder
- Support for α blending of Background, Video display, Still, OSD, and Cursor planes, 256-level transparency adaptable
- Adjustable saturation, contrast, brightness
- 10-bit RGB/YCbCr resolution
- YUV, RGB, CVBS and S-Video output modes

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- Output standard, NTSC or PAL
- Integrated 4-channel video DAC, supporting 2-channel CVBS and single channel component (YCbCr/RGB/S-Video) output

MDDRC & SSMC

- 144/133 MHz, 16-bit data line operation mode
- SDRAM/DDR controller
- SDRAM/DDR with 8 MB to 64 MB memory capacity
- 2D graphics acceleration
- Two 16 MB Flash banks
- ISA bus peripheral extension

Peripheral Interfaces

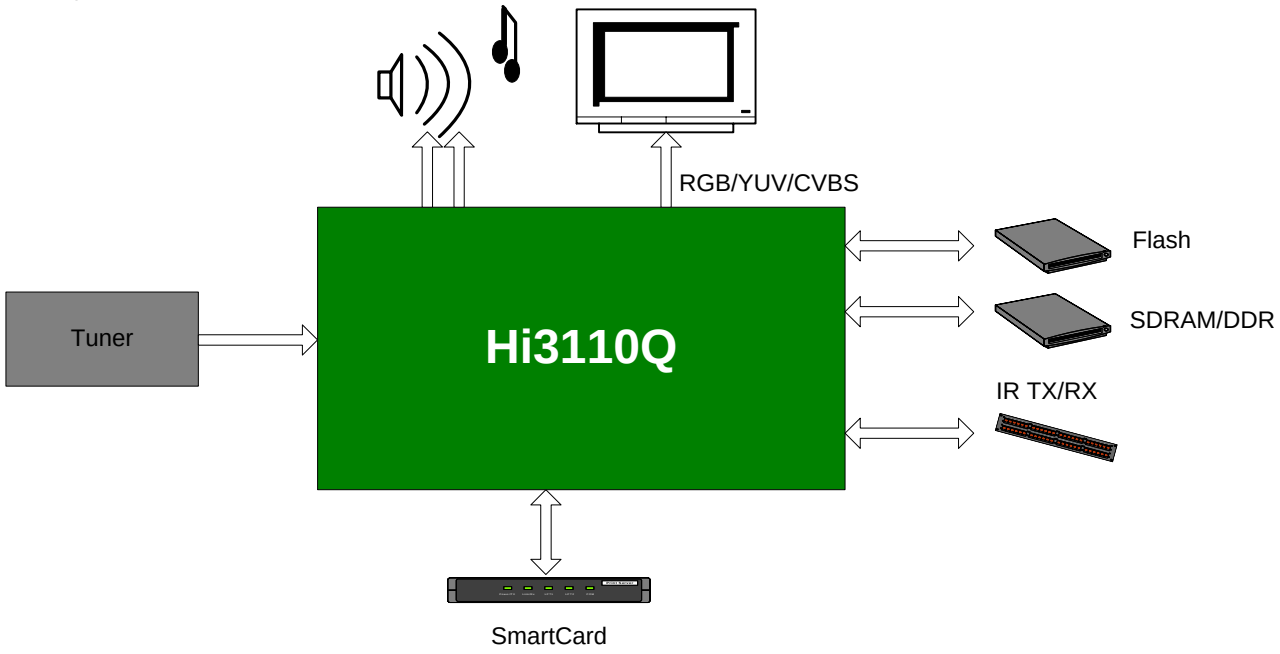
- One UART interface, up to 460.8 kbit/s, support for Modem function
- One smart card interface, supporting the asynchronous T0, T1,T14 (Irdeto) transport protocol
- One Infrared receive interface
- Four LED control module interfaces
- Two independent GPIO interfaces
- Two I^2C interfaces for interface control
- Four timers, one watchdog and one RTC
- One-channel pulse width modulation (PWM) control signals

Basic Features

- Typical power consumption of 1.0 W
- Four power-saving modes: IDLE, SLEEP, DOZE and NORMAL
- 0.13 µm technology, 1.2/3.3/2.5 V chip power voltage
- PQFP208 package
- Working temperature: 0°C to +70°C

Applications and the Typical Application Diagram

- Digital video broadcasting set-top box
- Digital TV set



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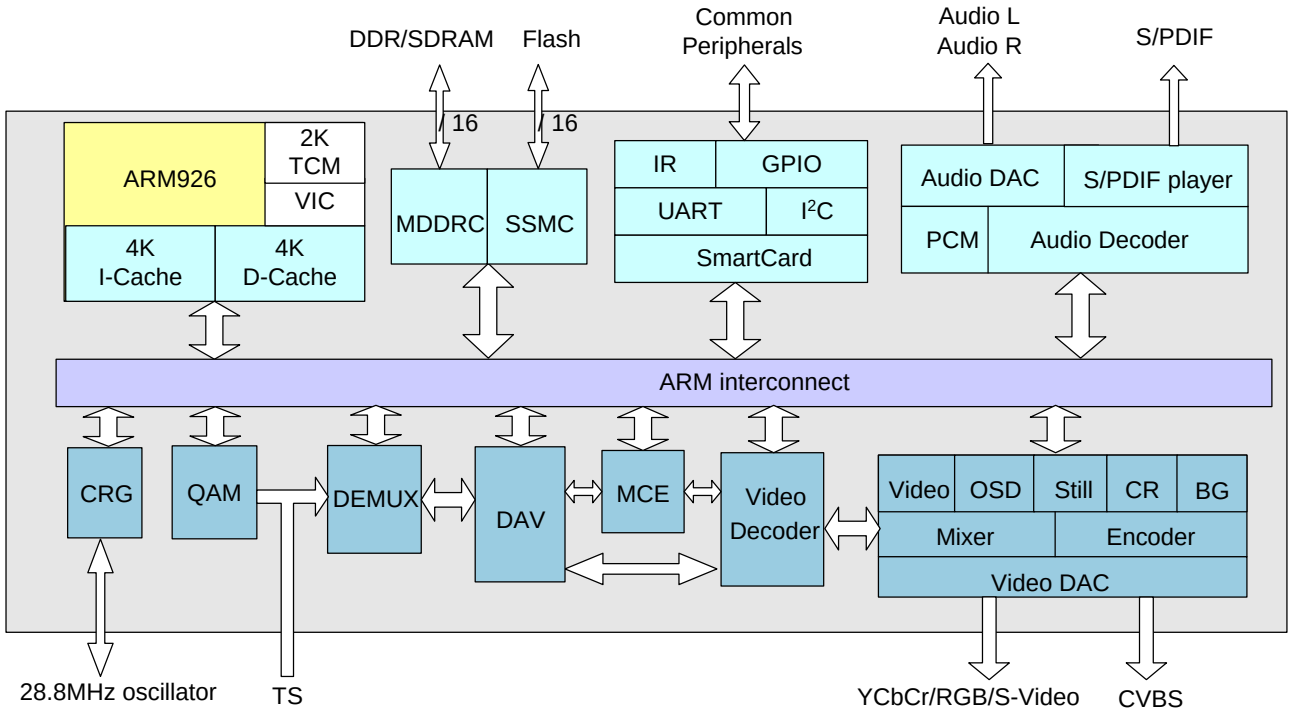
Block Diagram



The Hi3110Q is a SoC chip that integrates the Quadrature Amplitude Modulation (QAM) demodulation and MPEG-2 source decoding functions. It offers a highly cost-effective DVB-C system solution and an excellent integrated machine solution in the industry.

The Hi3110Q integrates a QAM demodulation module and provides powerful 16/32/64/128/256-QAM demodulation, as well as RS forward error correction. It is intended for the complete processing toward cable TV signals, from IF sample to MPEG-TS output. Thus it offers solutions for digital transmission of TV, audio and data signals over coaxial cables.

The Hi3110Q integrates an ARM926EJ-S core whose main frequency is up to 252 MHz, which supports 4 KB I/D-Cache and 2 KB ITCM. The Hi3110Q provides the following external interfaces:

- MDDRC: selects the SDRAM/DDR storage mode and provides more flexibility for users.
- SSMC: supports Flash and the Industry Standard Architecture (ISA) bus peripheral extension

The Hi3110Q supports the following functions:

- MPEG-2 MP@ML video decoding
- Downward compatibility with MPEG-1 decoding
- Multi-level error tolerance
- Video scaling with programmable ratio
- MPEG-2 layer I/II and MPEG-1 layer I/II audio decoding
- Five-layer overlay display, including Background, Video, Still, On-Screen Display (OSD) and Cursor

The Hi3110Q provides the following interfaces:

- Analog video output interfaces
- Analog audio interfaces
- S/PDIF digital interfaces

In addition, the Hi3110Q also supports general-purpose peripherals such as I^2C, smart card, Infrared Remoter (IR), and UART for implementing interactive functions.

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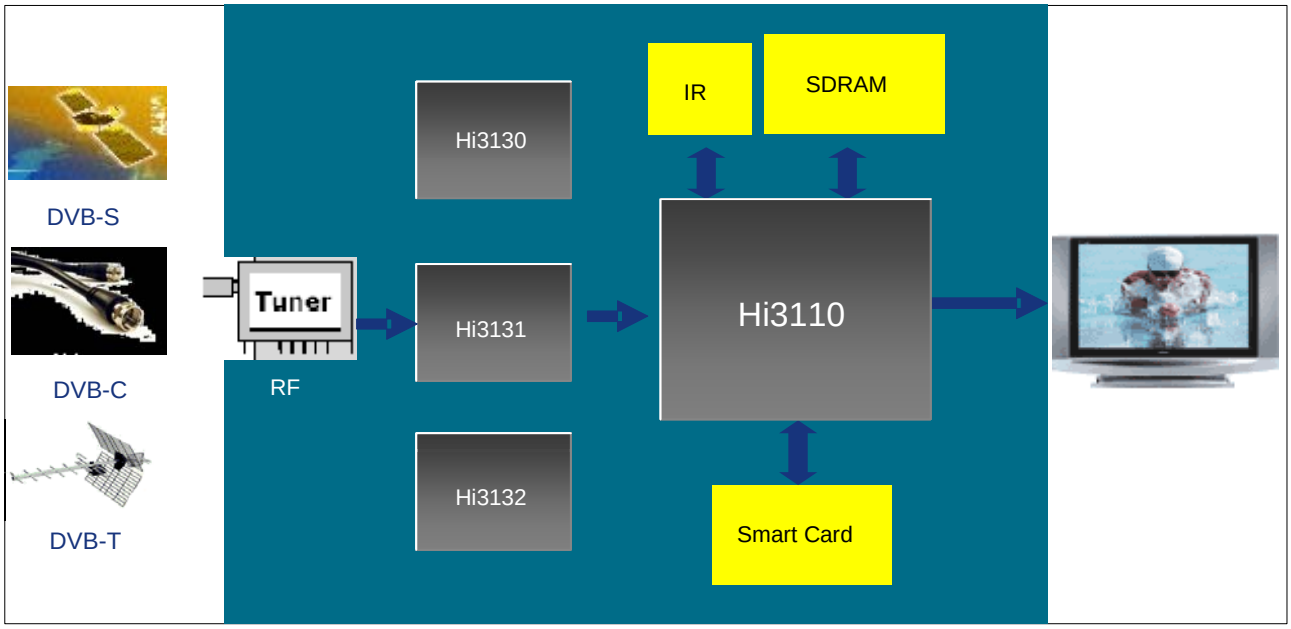
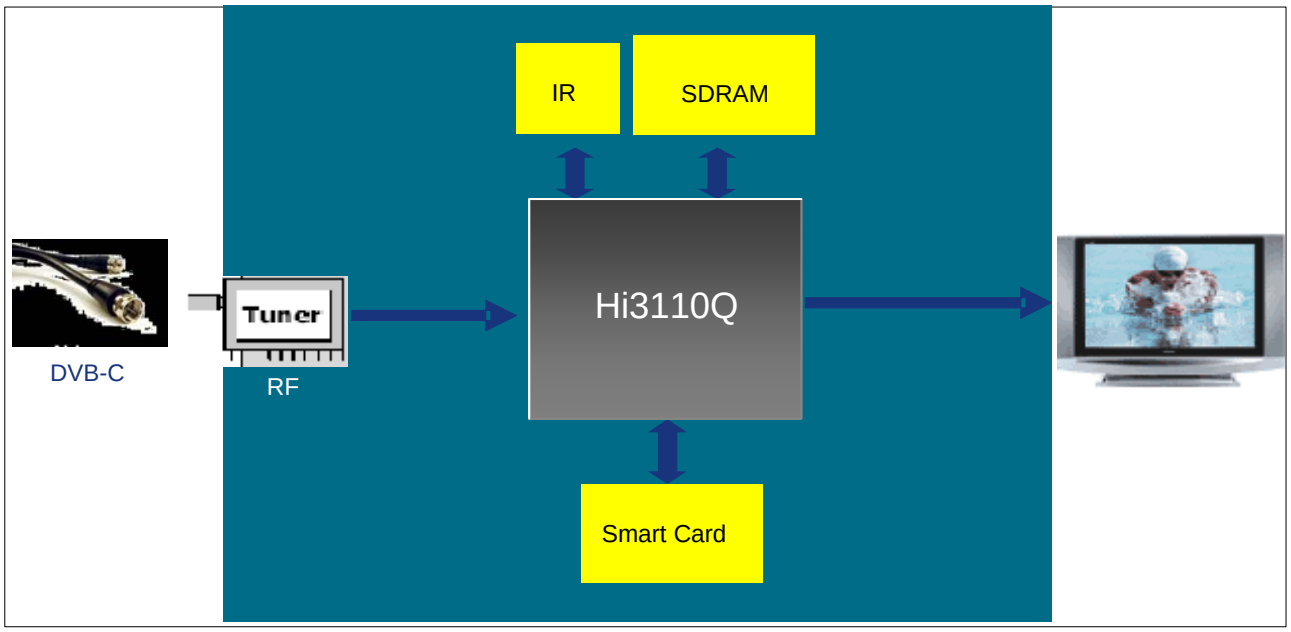
Hi3110QV100 Demodulating and Decoding Chip

HI311x−DVB STB Solution

The Hi3110 is a high-performance SoC chip that provides the MPEG-2 source decoding functions. It can be widely used in set-top boxes of DVB-C, DVB-S, and DVB-T.



The Hi3110Q is a high-performance SoC chip that provides the MPEG-2 source decoding functions and integrates a QAM demodulator. It offers a low-cost cable digital TV set-top box solution.



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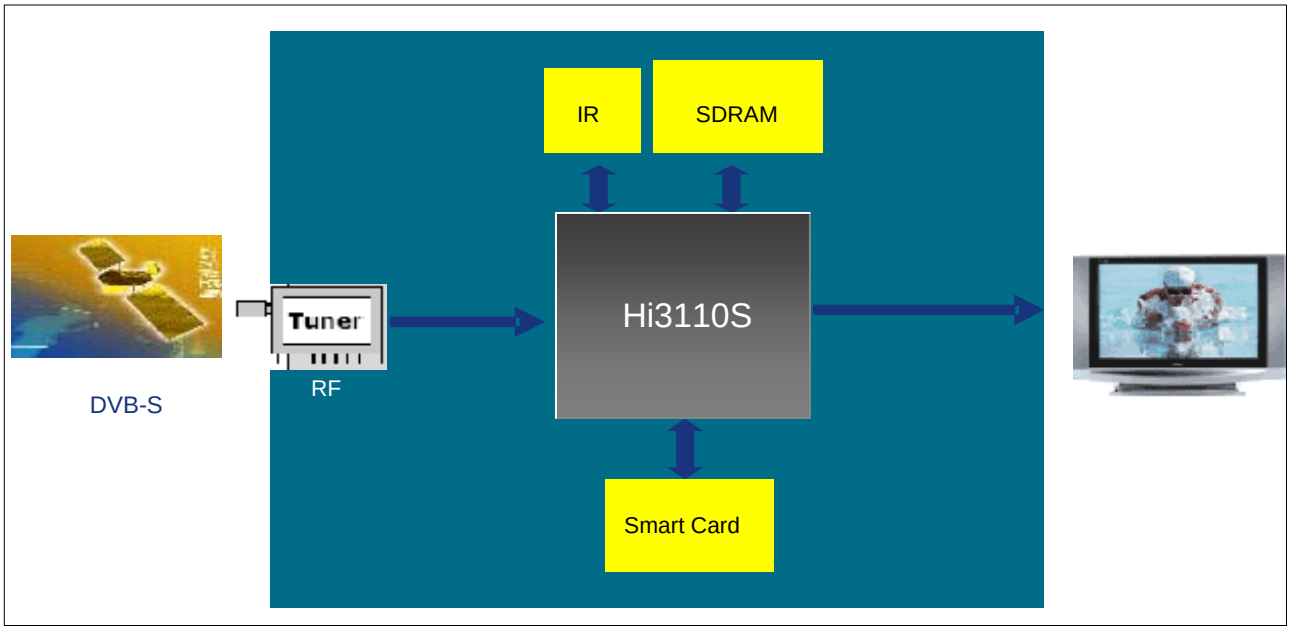
Hi3110QV100 Demodulating and Decoding Chip

The Hi3110S is a high-performance SoC chip that provides the MPEG-2 source decoding functions and integrates a QPSK demodulator. It offers a low-cost satellite digital TV set-top box solution.



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